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DECLARATION

I, Michie Fuse-Ofuchi , a Patent Attorney, of Ogikubo TM Bldg. 2F, 5-26-13, Ogikubo, Suginami-ku, Tokyo 167-0051, Japan, solemnly and sincerely declare:

That I have a thorough knowledge of Japanese and English languages; and

That the attached pages contain a correct translation into English of the specification of the following Japanese Patent Application:

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[Title of the Invention] SEMICONDUCTOR DEVICE, MEMORY SYSTEM AND ELECTRONIC APPARATUS

[Claims]

[Claim 1] A semiconductor device provided with a memory cell including a first driver transistor, a second driver transistor, a first transfer transistor, a second transfer transistor, a first load transistor and a second load transistor, the semiconductor device comprising:

a first gate-gate electrode layer including a gate electrode of the first load transistor and a gate electrode of the first driver transistor;

a second gate-gate electrode layer including a gate electrode of the second load transistor and a gate electrode of the second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer;

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer; and

a first active region in which the first load transistor is provided,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and

wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region.

[Claim 2] The semiconductor device according to claim 1, wherein the first

protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors are provided.

[Claim 3] The semiconductor device according to claim 1 or 2, wherein a part of the first active region and the first protruded active region form an L-shape.

[Claim 4] The semiconductor device according to any one of claims 1 to 3, comprises:

a second active region in which the second load transistor is provided; and

a second protruded active region provided in a manner to protrude from an end portion of the second active region.

[Claim 5] The semiconductor device according to claim 4, wherein the second protruded active region is provided in a manner to protrude on a side opposite to a side where the first and second driver transistors are provided.

[Claim 6] The semiconductor device according to claim 4 or 5, wherein a part of the second active region and the second protruded active region form an L-shape.

[Claim 7] The semiconductor device according to any one of claims 1 to 6,

wherein the first drain-gate wiring layer is electrically connected to the second drain-drain wiring layer through a contact section, and

wherein the second drain-gate wiring layer is electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

[Claim 8] The semiconductor device according to any one of claims 1 to 7, wherein the first drain-gate wiring layer is located in a layer lower than the second drain-gate wiring layer.

[Claim 9] The semiconductor device according to any one of claims 1 to 8, wherein the first drain-gate wiring layer is located in a layer in which the first gate-gate electrode layer is provided.

[Claim 10] The semiconductor device according to any one of claims 1 to 9, wherein the second drain-gate wiring layer is formed across a plurality of layers.

[Claim 11] The semiconductor device according to claim 10,

wherein the second drain-gate wiring layer includes a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and

wherein the upper layer is located in a layer over the lower layer, and electrically connected to the lower layer.

[Claim 12] The semiconductor device according to claim 11, wherein the upper layer is electrically connected to the lower layer through a contact section.

[Claim 13] The semiconductor device according to claim 11 or 12,

wherein the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer are located in the first conductive layer,

wherein the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer are located in the second conductive layer, and

wherein the upper layer is located in the third conductive layer.

[Claim 14] The semiconductor device according to any one of claims 1 to 13, wherein the second conductive layer is a nitride layer of a refractory metal.

[Claim 15] The semiconductor device according to any one of claims 1 to 14, wherein the second conductive layer has a thickness of 100 nm to 200 nm.

[Claim 16] A semiconductor device using as a memory cell a flip-flop including a first load transistor, a first driver transistor, a second load transistor and a second driver transistor,

wherein the first and second load transistors in one memory cell are disposed symmetrically about a straight line extending in a gate width direction between drain regions of the first and second load transistors, and

wherein each of the drain regions of the first and second load transistors includes a protruded active region protruding in the gate width direction beyond an end of a channel region.

[Claim 17] A memory system provided with the semiconductor device defined in any one of claims 1 to 16.

[Claim 18] An electronic apparatus provided with the semiconductor device defined in any one of claims 1 to 16.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to semiconductor devices, such as, for example, static random access memories (SRAMs), and memory systems and electronic apparatuses provided with the same.

[0002]

[Background Art]

SRAMs, one type of semiconductor memory devices, do not require a refreshing operation and therefore have a property that can simplify the system and lower power consumption. For this reason, the SRAMs are prevailingly used as memories for electronic equipment, such as, for example, mobile phones.

[0003]

[Problems to be Solved by the Invention]

The objective of the present invention is to provide a semiconductor device that can reduce its cell area.

[0004]

Another objective of the present invention is to provide a memory system and an electronic apparatus that includes a semiconductor device of the present invention.

[0005]

[Means for Solving the Problems]

1. Semiconductor Device

1.1 First Semiconductor Device

A semiconductor device in accordance with the present invention is provided with a memory cell including a first driver transistor, a second driver transistor, a first transfer transistor, a second transfer transistor, a first load transistor and a second load transistor, and the semiconductor device comprises:

a first gate-gate electrode layer including a gate electrode of the first load transistor and a

gate electrode of the first driver transistor;

a second gate-gate electrode layer including a gate electrode of the second load transistor and a gate electrode of the second driver transistor;

a first drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the first load transistor and a drain region of the first driver transistor;

a second drain-drain wiring layer which forms a part of a connection layer that electrically connects a drain region of the second load transistor and a drain region of the second driver transistor;

a first drain-gate wiring layer which forms a part of a connection layer that electrically connects the first gate-gate electrode layer and the second drain-drain wiring layer;

a second drain-gate wiring layer which forms a part of a connection layer that electrically connects the second gate-gate electrode layer and the first drain-drain wiring layer; and

a first active region in which the first load transistor is provided,

wherein the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively, and

wherein a first protruded active region is provided in a manner to protrude from an end portion of the first active region.

[0006]

Here, the "wiring layer" means a conductive layer disposed over a field or an interlayer dielectric layer.

[0007]

In accordance with the present invention, the second drain-gate wiring layer is located above the first drain-gate wiring layer. In other words, the first drain-gate wiring layer and the second drain-gate wiring layer are located in different layers, respectively. As a result, in accordance with the present invention, the pattern density of a wiring layer in each of the layers where the first drain-gate wiring layer and the second drain-gate wiring layer are formed, respectively, can be reduced and the cell area can be made smaller, compared to the case where the first drain-gate wiring layer and the second drain-gate wiring layer are formed in the same layer.

[0008]

Further, in accordance with the present invention, the first protruded active region is provided in a manner to protrude from an end portion of the first active region. As a result, for example, contacting area between the drain region of the first load transistor provided in the first active region and a contact section provided in an interlayer dielectric layer can be secured, and their contact resistance can be restrained from increasing. The reasons for this will be described later in the description of embodiments of the present invention.

[0009]

The semiconductor device of the present invention may take at least any one of the following features.

[0010]

(A) The first protruded active region may be provided in a manner to protrude on a side opposite to a side where the first and second driver transistors are provided. According to this feature, the first protruded active region can be prevented from reaching a well region in which the first and second driver transistors are provided.

[0011]

(B) A part of the first active region and the first protruded active region may form an L-shape.

[0012]

(C) The semiconductor device may comprise a second active region in which the second load transistor is provided; and a second protruded active region provided in a manner to protrude from an end portion of the second active region. In accordance with this feature, for example, contacting area between the drain region of the second load transistor provided in the second active region and a contact section provided in an interlayer dielectric layer can be secured, and their contact resistance can be restrained from increasing. The reasons for this will be described later in the description of embodiments of the present invention.

[0013]

In the feature of (C), the second protruded active region may be provided in a manner to

protrude on a side opposite to a side where the first and second driver transistors are provided. According to this feature, the second protruded active region is prevented from reaching a well region in which the first and second driver transistors are provided.

[0014]

Further, in the feature of (C), a part of the second active region and the second protruded active region may form an L-shape.

[0015]

(D) The first drain-gate wiring layer may be electrically connected to the second drain-drain wiring layer through a contact section, and

the second drain-gate wiring layer may be electrically connected to the second gate-gate electrode layer through a contact section, and electrically connected to the first drain-drain wiring layer through a contact section.

[0016]

(E) The first drain-gate wiring layer may be located in a layer lower than the second drain-gate wiring layer.

[0017]

(F) The first drain-gate wiring layer may be located in a layer in which the first gate-gate electrode layer is provided.

[0018]

(G) The second drain-gate wiring layer may be formed across a plurality of layers.

[0019]

In the feature of (G), the second drain-gate wiring layer may include a lower layer of the second drain-gate wiring layer and an upper layer of the second drain-gate wiring layer, and

the upper layer may be located in a layer over the lower layer, and electrically connected to the lower layer.

[0020]

Further, in the feature of (G), the upper layer may be electrically connected to the lower layer through a contact section.

[0021]

Further, in the feature of (G), the first gate-gate electrode layer, the second gate-gate electrode layer and the first drain-gate wiring layer may be located in the first conductive layer,

the first drain-drain wiring layer, the second drain-drain wiring layer and the lower layer may be located in the second conductive layer, and

the upper layer may be located in the third conductive layer.

[0022]

(H) The second conductive layer may be a nitride layer of a refractory metal (for example, titanium nitride). As the second conductive layer is a nitride layer of a refractory metal, the thickness of the second conductive layer can be reduced, and miniaturizing processing can be readily performed. Accordingly, the cell area can be reduced.

[0023]

(I) The second conductive layer may have a thickness of 100 nm to 200 nm.

[0024]

1.2 Second Semiconductor Device

A semiconductor device in accordance with the present invention uses as a memory cell a flip-flop including a first load transistor, a first driver transistor, a second load transistor and a second driver transistor,

wherein the first and second load transistors in one memory cell are disposed symmetrically about a straight line extending in a gate width direction between drain regions of the first and second load transistors, and

wherein each of the drain regions of the first and second load transistors includes a protruded active region protruding in the gate width direction beyond an end of a channel region.

[0025]

It is noted that, in the present invention, each of the drain regions includes a protruded active region protruding in the gate width direction beyond an end of a channel region. As a result, for example, contacting area between the drain region of the first load transistor and a contact section provided in an interlayer dielectric layer can be secured, and their contact

resistance can be restrained from increasing. The reasons for this will be described later in the description of embodiments of the invention.

[0026]

2. Memory System

A memory system in accordance with the present invention is provided with the semiconductor device in accordance with the present invention.

[0027]

3. Electronic Apparatus

An electronic apparatus in accordance with the present invention is provided with the semiconductor device in accordance with the present invention.

[0028]

[Embodiments]

An embodiment of the present invention is described. The present embodiment is the one in which a semiconductor device of the present invention is applied to in an SRAM.

[0029]

1. Equivalent Circuit of SRAM

Fig. 1 shows a relationship between an equivalent circuit of an SRAM in accordance with the present embodiment and corresponding conductive layers. The SRAM of the present embodiment is a type in which one memory cell is formed with six MOS field effect transistors. In other words, one CMOS inverter is formed with an n-channel type driver transistor Q3 and a p-channel type load transistor Q5. Also, one CMOS inverter is formed with an n-channel type driver transistor Q4 and a p-channel type load transistor Q6. These two CMOS inverters are cross-coupled to form a flip-flop. Further, one memory cell is formed from this flip-flop and n-channel type transfer transistors Q1 and Q2.

[0030]

2. Structure of SRAM

A structure of the SRAM is described below. First, each figure is briefly described.

[0031]

Fig. 1 shows a relationship between an equivalent circuit of an SRAM in accordance with the present embodiment and corresponding conductive layers. Fig. 2 schematically shows a plan view of a field of the memory cell of the SRAM in accordance with the present embodiment. Fig. 3 schematically shows a plan view of a first conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 4 schematically shows a plan view of a second conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 5 schematically shows a plan view of a third conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 6 schematically shows a plan view of a fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 7 schematically shows a plan view of the field and the first conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 8 schematically shows a plan view of the field and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 9 schematically shows a plan view of the first conductive layer and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 10 schematically shows a plan view of the second conductive layer and the third conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 11 schematically shows a plan view of the third conductive layer and the fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment. Fig. 12 schematically shows a cross-sectional view taken along a line A-A shown in Fig. 2 to Fig. 11. Fig. 13 schematically shows a cross-sectional view taken along a line B-B shown in Fig. 2 to Fig. 11.

[0032]

The SRAM is formed including an element forming region formed in a field, a first conductive layer, a second conductive layer, a third conductive layer, and a fourth conductive layer. The structure of each of the field, and the first through fourth conductive layers is concretely described below.

[0033]

2.1 Field

Referring to Fig. 2, the field is described. The field includes first through fourth active regions 14, 15, 16 and 17, first and second protruded active regions 18 and 19 and an element isolation region 12. The first through fourth active regions 14, 15, 16 and 17 and the first and second protruded active regions 18 and 19 are defined by the element isolation region 12. A region on the side where the first and second active regions 14 and 15 and the first and second protruded active regions 18 and 19 are formed is an n-type well region W10, and a region on the side where the third and fourth active regions 16 and 17 are formed is a p-type well region W20.

[0034]

The first active region 14 and the first protruded active region 18, and the second active region 15 and the second protruded active region 19 are disposed in a symmetrical relation in a planar configuration. Also, the third active region 16 and the fourth active region 17 are disposed in a symmetrical relation in a planar configuration.

[0035]

The first protruded active region 18 is provided in a manner to protrude from an end portion of the first active region 14. More concretely, the first protruded active region 18 may be provided in a manner to protrude toward a side opposite to the side where the p-well region W20 is formed. Also, a part of the first active region 14 and the first protruded active region 18 may form an L-shape. The first protruded active region 18 has a length L10, which is, for example, 0.14 μm to 0.20 μm. The first protruded active region 18 has a width W10, which is, for example, 0.18 μm to 0.22 μm. Effects provided by the provision of the first protruded active region 18 will be described below in section "Effects".

[0036]

The second protruded active region 19 is provided in a manner to protrude from an end portion of the second active region 15. More concretely, the second protruded active region 19 may be provided in a manner to protrude toward a side opposite to the side where the p-well region W20 is formed. Also, a part of the second active region 15 and the second protruded active region 19 may form an L-shape. The second protruded active region 19 has a length L20, which is, for example, 0.14 μm to 0.20 μm. The second protruded active region 19 has a width

W20, which is, for example, 0.18 μm to 0.22 μm. Effects provided by the provision of the second protruded active region 19 will be described below in section "Effects".

[0037]

The first load transistor Q5 is formed in the first active region 14 and the first protruded active region 18. In the first active region 14, a first p^+-type impurity layer 14a is formed. In the first active region 14 and the first protruded active region 18, a second p^+-type impurity layer 14b is formed. The first p^+-type impurity layer 14a functions as a source of the first load transistor Q5. The second p^+-type impurity layer 14b functions as a drain of the first load transistor Q5.

[0038]

The second load transistor Q6 is formed in the second active region 15 and the second protruded active region 19. In the second active region 15, a third p^+-type impurity layer 15a is formed. In the second active region 15 and the second protruded active region 19, a fourth p^+-type impurity layer 15b is formed. The third p^+-type impurity layer 15a functions as a source of the second load transistor Q6. The fourth p^+-type impurity layer 15b functions as a drain of the second load transistor Q6.

[0039]

In the third active region 16, the first driver transistor Q3 and the first transfer transistor Q1 are formed. In the third active region 16, first through third n^+-type impurity layers 16a, 16b and 16c that are to become components of the transistors Q1 and Q3, and a fifth p^+-type impurity layer 16d that composes a well contact region are formed. The first n^+-type impurity layer 16a functions as a source or a drain of the first transfer transistor Q1. The second n^+-type impurity layer 16b functions as a drain of the first driver transistor Q3 and a source or a drain of the first transfer transistor Q1. The third n^+-type impurity layer 16c functions as a source of the first driver transistor Q3.

[0040]

In the fourth active region 17, the second driver transistor Q4 and the second transfer transistor Q2 are formed. In the fourth active region 17, fourth through sixth n^+-type impurity

layers 17a, 17b and 17c that are to become components of the transistors Q2 and Q4, and a sixth p^+-type impurity layer 17d that composes a well contact region are formed. The fourth n^+-type impurity layer 17a functions as a source or a drain of the second transfer transistor Q2. The fifth n^+-type impurity layer 17b functions as a drain of the second driver transistor Q4 and a source or a drain of the second transfer transistor Q2. The sixth n^+-type impurity layer 17c functions as a source of the second driver transistor Q4.

[0041]

2.2 First Conductive Layer

Next, referring to Fig. 3 and Fig. 7, the first conductive layer is described. It is noted that the first conductive layer means a conductive layer that is formed on the field 10.

[0042]

The first conductive layer includes a first gate-gate electrode layer 20, a second gate-gate electrode layer 22, a first drain-gate wiring layer 30 and an auxiliary word line 24.

[0043]

The first gate-gate electrode layer 20 and the second gate-gate electrode layer 22 are formed in a manner to extend along a Y direction. The first drain-gate wiring layer 30 and the auxiliary word line 24 are formed in a manner to extend along an X direction.

[0044]

Components of the first conductive layer are described concretely below.

[0045]

1) First Gate-Gate Electrode Layer

The first gate-gate electrode layer 20 is formed in a manner to traverse the first active region 14 and the third active region 16, as shown in Fig. 7. The first gate-gate electrode layer 20 functions as a gate electrode of the first load transistor Q5 and the first driver transistor Q3.

[0046]

The first gate-gate electrode layer 20 is formed in a manner to pass between the first p^+-type impurity layer 14a and the second p^+-type impurity layer 14b, in the first active region 14. In other words, the first gate-gate electrode layer 20, the first p^+-type impurity layer 14a and the

second p^+-type impurity layer 14b form the first load transistor Q5. Also, the first gate-gate electrode layer 20 is formed in a manner to pass between the second n^+-type impurity layer 16a and the third n^+-type impurity layer 16c, in the third active region 16. In other words, the first gate-gate electrode layer 20, the second n^+-type impurity layer 16a and the third n^+-type impurity layer 16c form the first driver transistor Q3.

[0047]

2) First Drain-Gate Wiring Layer

The first drain-gate wiring layer 30 is formed in a manner to extend in the X direction from a side section of the first gate-gate electrode layer 20 toward the second gate-gate electrode layer 22. Also, as shown in Fig. 7, the first drain-gate wiring layer 30 is formed at least between the first active region 14 and the third active region 16.

[0048]

3) Second Gate-Gate Electrode Layer

The second gate-gate electrode layer 22 is formed in a manner to traverse the second active region 15 and the fourth active region 17, as shown in Fig. 7. The second gate-gate electrode layer 22 functions as a gate electrode of the second load transistor Q6 and the second driver transistor Q4.

[0049]

The second gate-gate electrode layer 22 is formed in a manner to pass between the third p^+-type impurity layer 15a and the fourth p^+-type impurity layer 15b, in the second active region 15. In other words, the second gate-gate electrode layer 22, the third p^+-type impurity layer 15a and the fourth p^+-type impurity layer 15b form the second load transistor Q6. Also, the second gate-gate electrode layer 22 is formed in a manner to pass between the fifth n^+-type impurity layer 17b and the sixth n^+-type impurity layer 17c, in the fourth active region 17. In other words, the second gate-gate electrode layer 22, the fifth n^+-type impurity layer 17b and the sixth n^+-type impurity layer 17c form the second driver transistor Q4.

[0050]

4) Auxiliary Word Line

The auxiliary word line 24 is formed in a manner to traverse the third active region 16 and the fourth active region 17, as shown in Fig. 7. The auxiliary word line 24 functions as a gate electrode of the first and second transfer transistors Q1 and Q2.

[0051]

The auxiliary word line 24 is formed in a manner to pass between the first n^+-type impurity layer 16a and the second n^+-type impurity layer 16b, in the third active region 16. In other words, the auxiliary word line 24, the first n^+-type impurity layer 16a and the second n^+-type impurity layer 16b form the first transfer transistor Q1. Also, the auxiliary word line 24 is formed in a manner to pass between the fourth n^+-type impurity layer 17a and the fifth n^+-type impurity layer 17b, in the fourth active region 17. In other words, the auxiliary word line 24, the fourth n^+-type impurity layer 17a and the fifth n^+-type impurity layer 17b form the second transfer transistor Q2.

[0052]

5) Cross-sectional Structure of First Conductive Layer and others

The first conductive layer may be formed by successively depositing a polysilicon layer and a silicide layer in layers, for example.

[0053]

As shown in Fig. 12 and Fig. 13, a first interlayer dielectric layer 90 is formed on the field and the first conductive layer. The first interlayer dielectric layer 90 may be formed through a planarization process utilizing, for example, a chemical mechanical polishing method.

[0054]

2.3 Second Conductive Layer

Referring to Fig. 4, Fig. 8 and Fig. 9, the second conductive layer is described below. It is noted that the second conductive layer means a conductive layer that is formed on the first interlayer dielectric layer 90.

[0055]

The second conductive layer includes, as shown in Fig. 4, a first drain-drain wiring layer 40, a second drain-drain wiring layer 42, a lower layer 32a of the second drain-gate wiring layer, a

first BL contact pad layer 70a, a first bar-BL contact pad layer 72a, a first Vss contact pad layer 74a and a Vdd contact pad layer 76.

[0056]

The first drain-drain wiring layer 40, the second drain-drain wiring layer 42 and the lower layer 32a of the second drain-gate wiring layer are formed in a manner to extend in the Y direction (the load transistor and the driver transistor). The first drain-drain wiring layer 40, the second drain-drain wiring layer 42 and the lower layer 32a of the second drain-gate wiring layer are successively disposed in the X direction.

[0057]

Components of the second conductive layer are concretely described below.

[0058]

1) First Drain-Drain Wiring Layer

The first drain-drain wiring layer 40 has portions that overlap the first active region 14 and the third active region 16 as viewed in a plan view (see Fig. 8). More concretely, one end portion 40a of the first drain-drain wiring layer 40 is located above the second p^+-type impurity layer 14b. The one end portion 40a of the first drain-drain wiring layer 40 and the second p^+-type impurity layer 14b are electrically connected to each other through a contact section between the field and the second conductive layer (herein blew referred to as a "field/second-layer contact section") 80. The other end portion 40b of the first drain-drain wiring layer 40 is located above the second n^+-type impurity layer 16b. The other end portion 40b of the first drain-drain wiring layer 40 and the second n^+-type impurity layer 16b are electrically connected to each other through the field/second-layer contact section 80.

[0059]

2) Second Drain-Drain Wiring Layer

The second drain-drain wiring layer 42 has portions that overlap the second active region 15 and the fourth active region 17 as viewed in a plan view (see Fig. 8). More concretely, one end portion 42a of the second drain-drain wiring layer 42 is located above the fourth p^+-type impurity layer 15b. The one end portion 42a of the second drain-drain wiring layer 42 and the

fourth p^+-type impurity layer 15b are electrically connected to each other through the field/second-layer contact section 80. The other end portion 42b of the second drain-drain wiring layer 42 is located above the fifth n^+-type impurity layer 17b. The other end portion 42b of the second drain-drain wiring layer 42 and the fifth n^+-type impurity layer 17b are electrically connected to each other through the field/second-layer contact section 80.

[0060]

Further, the second drain-drain wiring layer 42 has a portion that overlaps an end portion 30a of the first drain-gate wiring layer 30 as viewed in a plan view (see Fig. 9). The second drain-drain wiring layer 42 and the end portion 30a of the first drain-gate wiring layer 30 are electrically connected to each other through a contact section between the first conductive layer and the second conductive layer (hereafter referred to as a "first-layer/second-layer contact section") 82.

[0061]

3) Lower Layer of Second Drain-Gate Wiring Layer

The lower layer 32a of the second drain-gate wiring layer is formed on the opposite side of the first drain-drain wiring layer 40 with respect to the second drain-drain wiring layer 42 as being a reference. The lower layer 32a of the second drain-gate wiring layer has a portion that overlaps the second gate-gate electrode layer 22 as viewed in a plan view (see Fig. 9). The lower layer 32a of the second drain-gate wiring layer, and the second gate-gate electrode layer 22 are electrically connected to each other through the first-layer/second-layer contact section 82.

[0062]

4) First BL Contact Pad Layer

The first BL contact pad layer 70a is located above the first n^+-type impurity layer 16a in the third active region 16 (see Fig. 8). The first BL contact pad layer 70a and the first n^+-type impurity layer 16a are electrically connected to each other through the field/second-layer contact section 80.

[0063]

5) First Bar-BL Contact Pad Layer

The first bar-BL contact pad layer 72a is located above the fourth n^+-type impurity layer 17a in the fourth active region 17 (see Fig. 8). The first bar-BL contact pad layer 72a and the fourth n^+-type impurity layer 17a are electrically connected to each other through the field/second-layer contact section 80.

[0064]

6) First Vss Contact Pad Layer

The first Vss contact pad layers 74a are located above the sources of the driver transistors Q3 and Q4 (for example, the third n^+-type impurity layer 16c) and the well contact region (for example, the fifth p^+-type impurity layer 16d) (see Fig. 8). Each of the first Vss contact pad layers 74a is electrically connected to the source of each of the driver transistors Q3 and Q4 (for example, the third n^+-type impurity layer 16c) through the field/second-layer contact section 80. Also, the first Vss contact pad layer 74a is electrically connected to the well contact region (for example, the fourth p^+-type impurity layer 16d) through the field/second-layer contact section 80.

[0065]

7) Vdd Contact Pad Layer

Each of the Vdd contact pad layers 76 is located above the source (for example, the first p^+-type impurity layer 14a) of each of the load transistors Q5 and Q6. Each of the Vdd contact pad layers 76 is electrically connected to the source (for example, the first p^+-type impurity layer 14a) of each of the load transistors Q5 and Q6 through the field/second-layer contact section 80.

[0066]

8) Cross-Sectional Structure of Second Conductive Layer

Next, a cross-sectional structure of the second conductive layer is described with reference to Fig. 12 and Fig. 13. The second conductive layer may be formed only from, for example, a nitride layer of a refractory metal. The thickness of the second conductive layer may be for example 100 nm to 200 nm, and more specifically be 140 nm to 160 nm. The nitride layer of a refractory metal may be formed from, for example, titanium nitride. Because the second conductive layer is formed from a nitride layer of a refractory metal, the thickness of the second conductive layer can be made smaller, and miniature processing thereof can be readily conducted.

Accordingly, the cell area can be reduced.

[0067]

Also, the second conductive layer may be composed in either one of the following embodiments. 1) It may have a structure in which a nitride layer of a refractory metal is formed on a metal layer formed from a refractory metal. In this case, the metal layer formed from a refractory metal is an under-layer, and may be composed of a titanium layer, for example. Titanium nitride may be listed as a material of the nitride layer of a refractory metal. 2) The second conductive layer may be composed only of a metal layer of a refractory metal.

[0068]

Next, a cross-sectional structure of the field/second-layer contact section 80 is described with reference to Fig. 12 and Fig. 13. The field/second-layer contact section 80 is formed in a manner to fill a through hole 90a that is formed in the first interlayer dielectric layer 90. The field/second-layer contact section 80 includes a barrier layer 80a, and a plug 80b formed over the barrier layer 80a. Titanium and tungsten may be listed as material of the plugs. The barrier layer 80a may be formed from a metal layer of a refractory metal, and a nitride layer of a refractory metal formed over the metal layer. For example, titanium may be listed as material of the metal layer of a refractory metal. Titanium nitride, for example, may be listed as material of the nitride layer of a refractory metal.

[0069]

Next, a cross-sectional structure of the first-layer/second-layer contact section 82 is described with reference to Fig. 12 and Fig. 13. The first-layer/second-layer contact section 82 is formed in a manner to fill a through hole 90b that is formed in the first interlayer dielectric layer 90. The first-layer/second-layer contact section 82 may have the same structure as that of the field/second-layer contact section 80 described above.

[0070]

A second interlayer dielectric layer 92 is formed in a manner to cover the second conductive layer. The second interlayer dielectric layer 92 may be formed through a planarization process using, for example, a chemical mechanical polishing method.

[0071]

2.4 Third Conductive Layer

The third conductive layer is described below with reference to Fig. 5 and Fig. 10. It is noted that the third conductive layer means a conductive layer that is formed on the second interlayer dielectric layer 92 (see Fig. 12 and Fig. 13).

[0072]

The third conductive layer includes an upper layer 32b of the second drain-gate wiring layer, a main word line 50, a Vdd wiring 52, a second BL contact pad layer 70b, a second bar-BL contact pad layer 72b and a second Vss contact pad layer 74b.

[0073]

The upper layer 32b of the second drain-gate wiring layer, the main word line 50 and the Vdd wiring 53 are formed in a manner to extend along the X direction. The second BL contact pad layer 70b, the second bar-BL contact pad layer 72b and the second Vss contact pad layer 74b are formed in a manner to extend along the Y direction.

[0074]

Components of the third conductive layer are concretely described below.

[0075]

1) Upper Layer of The Second Drain-Gate Wiring Layer

The upper layer 32b of the second drain-gate wiring layer is formed in a manner to traverse the second drain-drain wiring layer 42 in the second conductive layer, as shown in Fig. 10. More concretely, the upper layer 32b of the second drain-gate wiring layer is formed from an area above the end portion 40b of the first drain-drain wiring layer 40 to an area above an end portion 32a1 of the lower layer 32a of the second drain-gate wiring layer. The upper layer 32b of the second drain-gate wiring layer is electrically connected to the end portion 40b of the first drain-drain wiring layer 40 through a contact section between the second conductive layer and the third conductive layer (herein after referred to as a "second-layer/third-layer contact section") 84. Also, the upper layer 32b of the second drain-gate wiring layer is electrically connected to the end portion 32a1 of the lower layer 32a of the second drain-gate wiring layer through the

second-layer/third-layer contact section 84.

[0076]

As shown in Fig. 1, the first drain-drain wiring layer 40 in the second conductive layer and the second gate-gate electrode layer 22 in the first conductive layer are electrically connected to each other through the second-layer/third-layer contact section 84, the upper layer 32b of the second gate-drain wiring layer, the second-layer/third-layer contact section 84, the lower layer 32a of the second gate-drain wiring layer, and the first-layer/second-layer contact section 82.

[0077]

2) Vdd Wiring

The Vdd wiring 52 is formed in a manner to pass over the Vdd contact pad layer 76, as shown in Fig. 10. The Vdd wiring 52 is electrically connected to the Vdd contact pad layer 76 through the second-layer/third-layer contact section 84.

[0078]

3) Second BL Contact Pad Layer

The second BL contact pad layer 70b is located above the first BL contact pad layer 70a. The second BL contact pad layer 70b is electrically connected to the first BL contact pad layer 70a through the second-layer/third-layer contact section 84.

[0079]

4) Second bar-BL Contact Pad Layer

The second bar-BL contact pad layer 72b is located above the first bar-BL contact pad layer 72a. The second bar-BL contact pad layer 72b is electrically connected to the first bar-BL contact pad layer 72a through the second-layer/third-layer contact section 84.

[0080]

5) Second Vss Contact Pad Layer

The second Vss contact pad layer 74b is located above the second Vss contact pad layer 74a. The second Vss contact pad layer 74b is electrically connected to the first Vss contact pad layer 74a through the second-layer/third-layer contact section 84.

[0081]

6) Cross-sectional structure of Third Conductive Layer

Next, a cross-sectional structure of the third conductive layer is described with reference to Fig. 12 and Fig. 13. The third conductive layer has a structure in which, for example, a nitride layer of a refractory metal, a metal layer, and a nitride layer of a refractory metal, in this order from the bottom, are successively stacked in layers. For example, titanium nitride may be listed as material of the nitride layer of a refractory metal. Aluminum, copper or an alloy of these metals, for example, may be listed as material of the metal layer.

[0082]

Next, a cross-sectional structure of the second-layer/third-layer contact section 84 is described. The second-layer/third-layer contact section 84 is formed in a manner to fill a through hole 92a formed in the second interlayer dielectric layer 92. The second-layer/third-layer contact section 84 may be provided with the same structure as that of the field/second-layer contact section 80 described above.

[0083]

A third interlayer dielectric layer 94 is formed in a manner to cover the third conductive layer. The third interlayer dielectric layer 94 may be formed through a planarization process using, for example a chemical mechanical polishing method.

[0084]

2.5 Fourth Conductive Layer

The fourth conductive layer is described below with reference to Fig. 6 and Fig. 11. It is noted that the fourth conductive layer means a conductive layer that is formed on the third interlayer dielectric layer 94.

[0085]

The fourth conductive layer includes a bit line 60, a bit-bar line 62 and a Vss wiring 64.

[0086]

The bit line 60, the bit-bar line 62 and the Vss wiring 64 are formed in a manner to extend along the Y direction.

[0087]

Compositions of the bit line 60, the bit-bar line 62 and the Vss wiring 64 are concretely described below.

[0088]

1) Bit Line

The bit line 60 is formed in a manner to pass over the second BL contact pad layer 70b, as shown in Fig. 11. The bit line 60 is electrically connected to the second BL contact pad layer 70b through a contact section between the third conductive layer and the fourth conductive layer (herein below referred to as a "third-layer/fourth-layer contact section") 86.

[0089]

2) Bar-Bit Line

The bit-bar line 62 is formed in a manner to pass over the second bar-BL contact pad layer 72b, as shown in Fig. 11. The bit-bar line 62 is electrically connected to the second bar-BL contact pad layer 72b through the third-layer/fourth-layer contact section 86.

[0090]

3) Vss Wiring

The Vss wiring 64 is formed in a manner to pass over the second Vss contact pad layer 74b, as shown in Fig. 11. The Vss wiring 64 is electrically connected to the second Vss contact pad layer 74b through the third-layer/fourth-layer contact section 86.

[0091]

4) Cross-Sectional Structure of Fourth Conductive Layer

Next, a cross-sectional structure of the fourth conductive layer is described with reference to Fig. 12 and Fig. 13. The fourth conductive layer may have the same structure as the structure of the third conductive layer described above.

[0092]

Next, a cross-sectional structure of the third-layer/fourth-layer contact section 86 is described. The third-layer/fourth-layer contact section 86 is formed in a manner to fill a through hole 94a that is formed in the third interlayer dielectric layer 94. The third-layer/fourth-layer contact section 86 may have the same structure as the structure of the field/second-layer contact

section 80 described above.

[0093]

Although not shown in Fig. 12 or Fig. 13, a passivation layer may be formed on the fourth conductive layer.

[0094]

3. Effects

Effects provided by the semiconductor device in accordance with the present embodiment are described below.

[0095]

(1) A first drain-gate wiring layer and a second drain-gate wiring layer could be formed in the same conductive layer. However, in this case, it is difficult to reduce the cell area due to the high pattern density of the conductive layer where the first and second drain-gate wiring layers are formed.

[0096]

However, in accordance with the present embodiment, the first drain-gate wiring layer 30 is located in the first conductive layer. Also, the second drain-gate wiring layer has a structure that is divided into the lower layer 32a of the second drain-gate wiring layer and the upper layer 32b of the second drain-gate wiring layer. The lower layer 32a of the second drain-gate wiring layer is located in the second conductive layer, and the upper layer 32b of the second drain-gate wiring layer is located in the third conductive layer. Consequently, the first drain-gate wiring layer and the second drain-gate wiring layer are formed in different layers, respectively. Accordingly, since the first drain-gate wiring layer and the second drain-gate wiring layer are not formed in the same layer, the pattern density of the wiring layer can be reduced. Therefore, by the memory cell in accordance with the present embodiment, the cell area can be reduced.

[0097]

(2) In the present embodiment, the first protruded active region 18 that protrudes from an end portion of the first active region 14 is provided. The resultant effects are described below.

[0098]

As an example for comparison, let us consider the case in which active regions 114 and 115 having a pattern shown in Fig. 17A are formed. In other words, let us consider the case in which protruded active regions that protrude from the end portions of the active regions 114 and 115 are not formed. When the active regions 114 and 115 are formed, their patterns are defined by a resist pattern. In the mean time, when a resist pattern having corner sections is formed, the resist pattern at the corner sections may be rounded due to the approximation effect. Accordingly, as shown in Fig. 17B, the active regions 114 and 115 may be formed with the patterns at corner sections C10, C20, C30 and C40 being rounded. When the corner sections C10, C20, C30 and C40 at the ends are rounded, the area of each of the active regions 114 and 115 is reduced accordingly. Therefore, contact areas between the impurity layers (for example, drain regions) 114b and 115b and the contact sections are reduced. As the contact areas are reduced, the contact resistance between the impurity layers 114b and 115b and the contact sections becomes greater.

[0099]

In accordance with the present embodiment, the first protruded active region 18 that protrudes from the end portion of the first active region 14 is provided. As a result, the first protruded active region 18 may be rounded due to the approximation effect, the first active region 14 is prevented from being rounded, and the reduction of the area of the first active region 14 can be prevented. Accordingly, the contact area between the impurity layer 14b and the contact section 80 can be securely provided. As a result, the contact resistance between the impurity layer 14b and the contact section 80 can be prevented from increasing.

[0100] Also, in accordance with the present embodiment, the second protruded active region 19 that protrudes from the end portion of the first active region 15 is provided. Therefore, for the same reasons as described above, the contact resistance between the impurity layer 15b and the contact section 80 can be prevented from increasing.

[0101]

(3) Also, in accordance with the present embodiment, the first and second protruded active regions 18 and 19 may be provided in a manner to protrude toward the sides opposite to the

sides where the p-well region W20. In other words, the first and second protruded active regions 18 and 19 may be provided in a manner to protrude toward the sides opposite to the sides where the driver transistors Q3 and Q4 are provided. In this case, the first and second protruded active regions 18 and 19 can be prevented from reaching the p-well region W20. Also, the first and second protruded active regions 18 and 19 are prevented from being short-circuited with the first drain-gate wiring layer 30.

[0102]

4. Example of Application of SRAM to Electronic Equipment

The SRAM in accordance with the present embodiment may be applied to electronic equipment, such as, for example, mobile equipment. Fig. 14 shows a block diagram of a part of a mobile telephone system. A CPU 540, an SRAM 550 and a DRAM 560 are mutually connected via a bus line. Further, the CPU 540 is connected to a keyboard 510 and an LCD driver 520 via the bus line. The LCD driver 520 is connected to a liquid crystal display section 530 via the bus line. The CPU 540, the SRAM 550 and the DRAM 560 compose a memory system.

[0103]

Fig. 15 shows a perspective view of a mobile telephone 600 that is provided with the mobile telephone system shown in Fig. 14. The mobile telephone 600 is equipped with a main body section 610 including a keyboard 612, a liquid crystal display section 614, a receiver section 616 and an antenna section 618, and a lid section 620 including a transmitter section 622.

[0104]

The present invention is not limited to the embodiment described above, and a variety of modifications can be made within the scope of the subject matter of the present invention.

[0105]

It is noted that, in the embodiment described above, the load transistor and the driver transistor on the left side are defined as the first load transistor and the first driver transistor, respectively. However, the load transistor and the driver transistor on the right side may be defined as the first load transistor and the first driver transistor, respectively.

[Brief Description of the Drawings]

[Fig.1]

Fig. 1 shows a relationship between an equivalent circuit of an SRAM in accordance with the present embodiment and corresponding conductive layers.

[Fig.2]

Fig. 2 schematically shows a plan view of a field of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.3]

Fig. 3 schematically shows a plan view of a first conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.4]

Fig. 4 schematically shows a plan view of a second conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.5]

Fig. 5 schematically shows a plan view of a third conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.6]

Fig. 6 schematically shows a plan view of a fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.7]

Fig. 7 schematically shows a plan view of the field and the first conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.8]

Fig. 8 schematically shows a plan view of the field and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.9]

Fig. 9 schematically shows a plan view of the first conductive layer and the second conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.10]

Fig. 10 schematically shows a plan view of the second conductive layer and the third conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.11]

Fig. 11 schematically shows a plan view of the third conductive layer and the fourth conductive layer of the memory cell of the SRAM in accordance with the present embodiment.

[Fig.12]

Fig. 12 schematically shows a cross-sectional view taken along a line A-A shown in Fig. 2 to Fig. 11.

[Fig.13]

Fig. 13 schematically shows a cross-sectional view taken along a line B-B shown in Fig. 2 to Fig. 11.

[Fig.14]

Fig. 14 shows a block diagram of a part of a mobile telephone system provided with the SRAM in accordance with the present embodiment.

[Fig.15]

Fig. 15 shows a perspective view of a mobile telephone that is provided with the mobile telephone system shown in Fig. 14.

[Fig.16]

Fig. 16 is an illustration to describe the effects of the present embodiment.

[Fig.17]

Fig. 17A schematically shows a plan view of a plane of an active region of an example for comparison, and Fig. 17B is an illustration to describe problems of the example for comparison.

[Explanation of Reference Numerals]

10 silicon substrate

12 element isolation region

14 first active region

14a, 14b p^+-type impurity layer

15 second active region

15a, 15b p^+-type impurity layer

16 third active region

16a, 16b, 16c n^+-type impurity layer

16d p^+-type impurity layer

17 fourth active region

17a, 17b, 17c n^+-type impurity layer

17d p^+-type impurity layer

18 first protruded active region

19 second protruded active region

20 first gate-gate electrode layer

22 second gate-gate electrode layer

24 auxiliary word line

30 first gate-drain wiring layer

32a lower layer of second gate-drain wiring layer

32b upper layer of second gate-drain wiring layer

40 first drain-drain wiring layer

42 second drain-drain wiring layer

50 main word line

52 Vdd wiring

60 bit line

62 bit-bar line

64 Vss wiring

70a first BL contact pad layer

70b second BL contact pad layer

72a first bar-BL contact pad layer

72b second bar-BL contact pad layer

74a first Vss contact pad layer

74b	second Vss contact pad layer
76	Vdd contact pad layer
80	field/second-layer contact section
82	first-layer/second-layer contact section
84	second-layer/third-layer contact section
86	third-layer/fourth-layer contact section
90	interlayer dielectric layer
90a	through hole
92	interlayer dielectric layer
92a	through hole
94	interlayer dielectric layer
94a	through hole
Q1	first transfer transistor
Q2	second transfer transistor
Q3	first driver transistor
Q4	second driver transistor
Q5	first load transistor
Q6	second load transistor

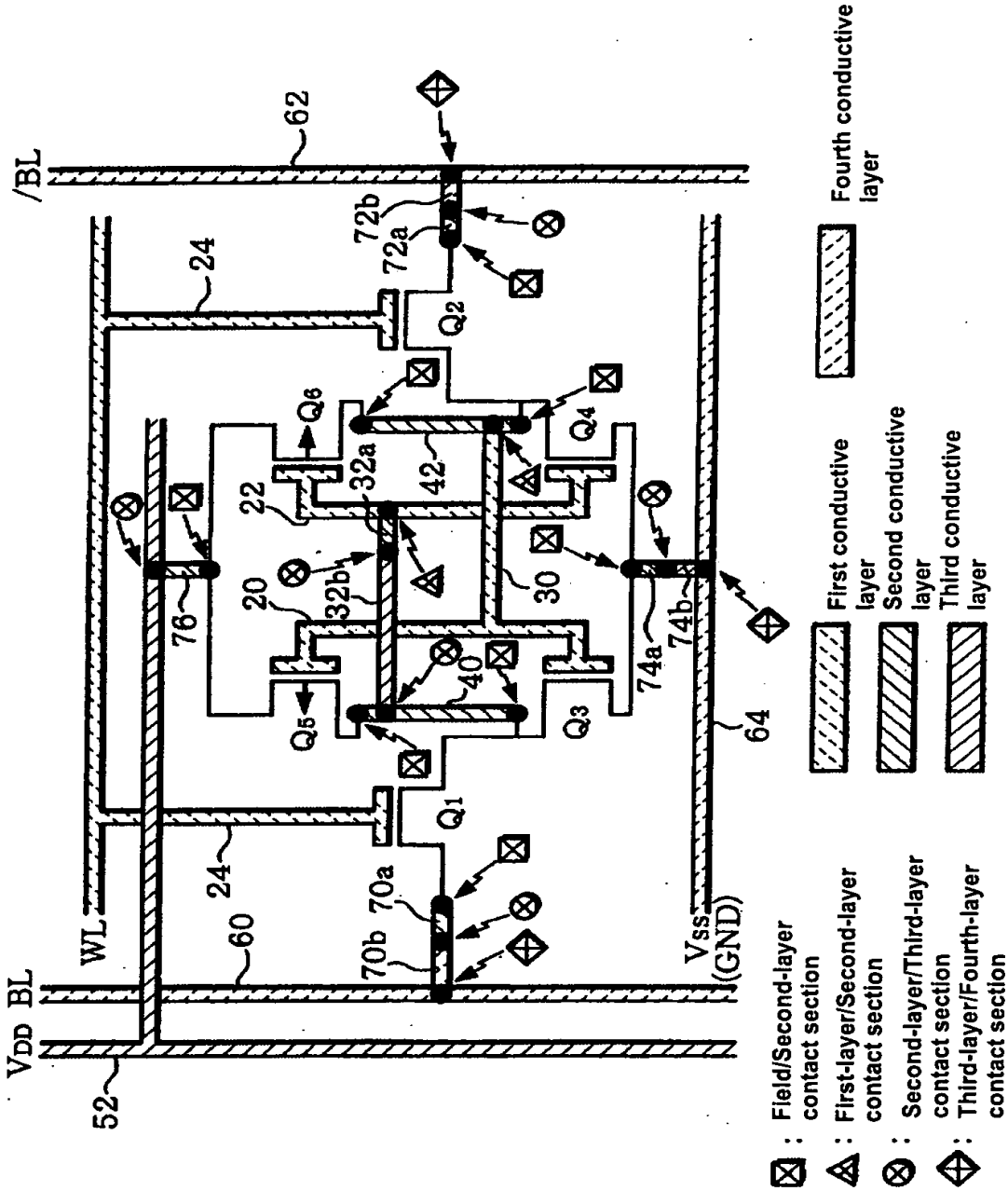

/BL
62
24
72b
72a
Q2
Q6
Q4
32a
42
22
20
32b
76
30
74b
74a
40
Q5
Q3
64
Q1
WL
24
70a
70b
60
VDD BL
52
Vss (GND)
Fourth conductive layer
First conductive layer
Second conductive layer
Third conductive layer
: Field/Second-layer contact section
: First-layer/Second-layer contact section
: Second-layer/Third-layer contact section
: Third-layer/Fourth-layer contact section

Fig. 1

Fig. 2

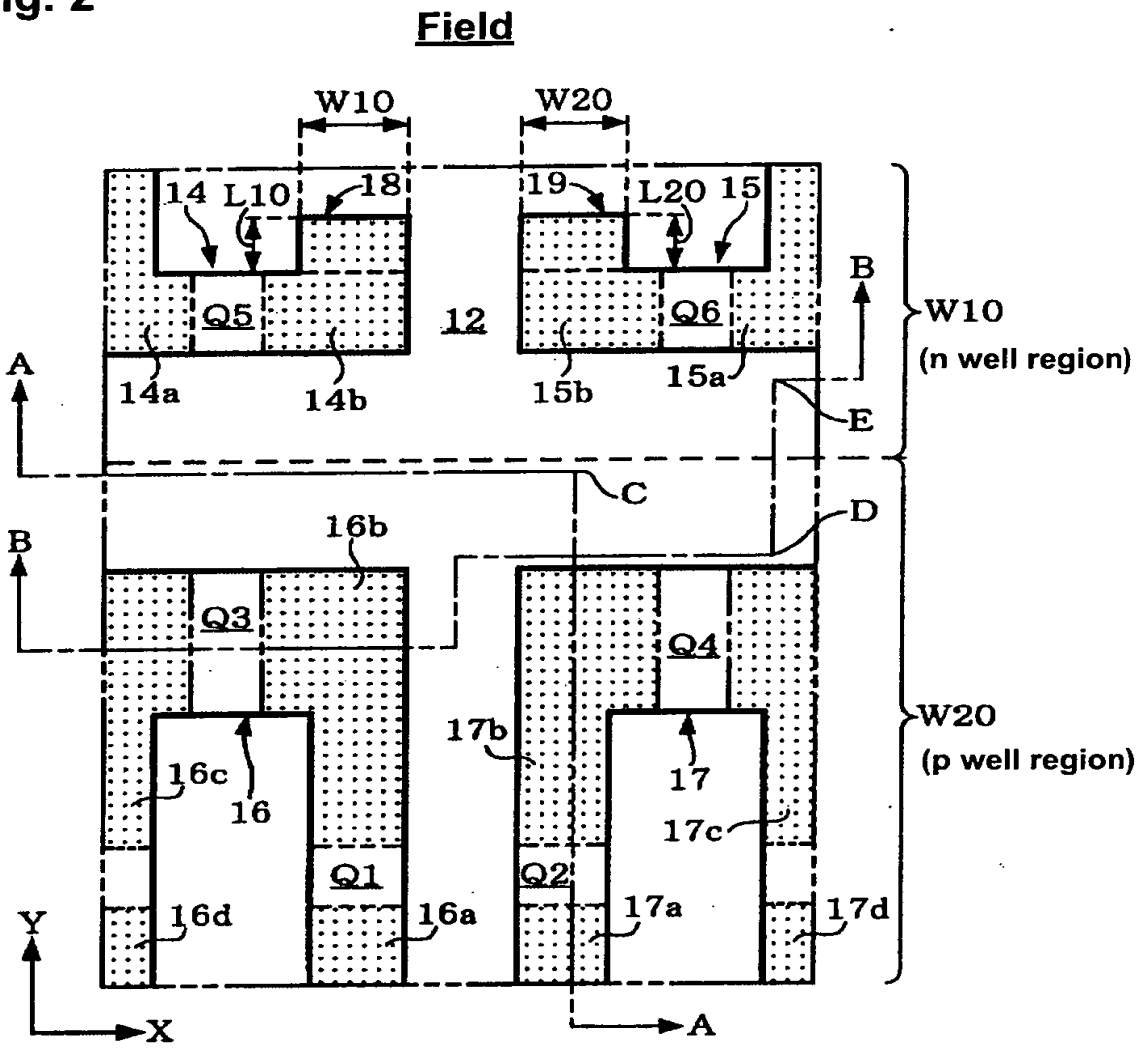

Field
W10
W20
14
L10
18
19
L20
15
B
Q5
12
Q6
W10
(n well region)
A
14a
14b
15b
15a
E
C
D
16b
B
Q3
Q4
W20
(p well region)
17b
16c
16
17
17c
Q1
Q2
16d
16a
17a
17d
Y
X
A

Fig. 3

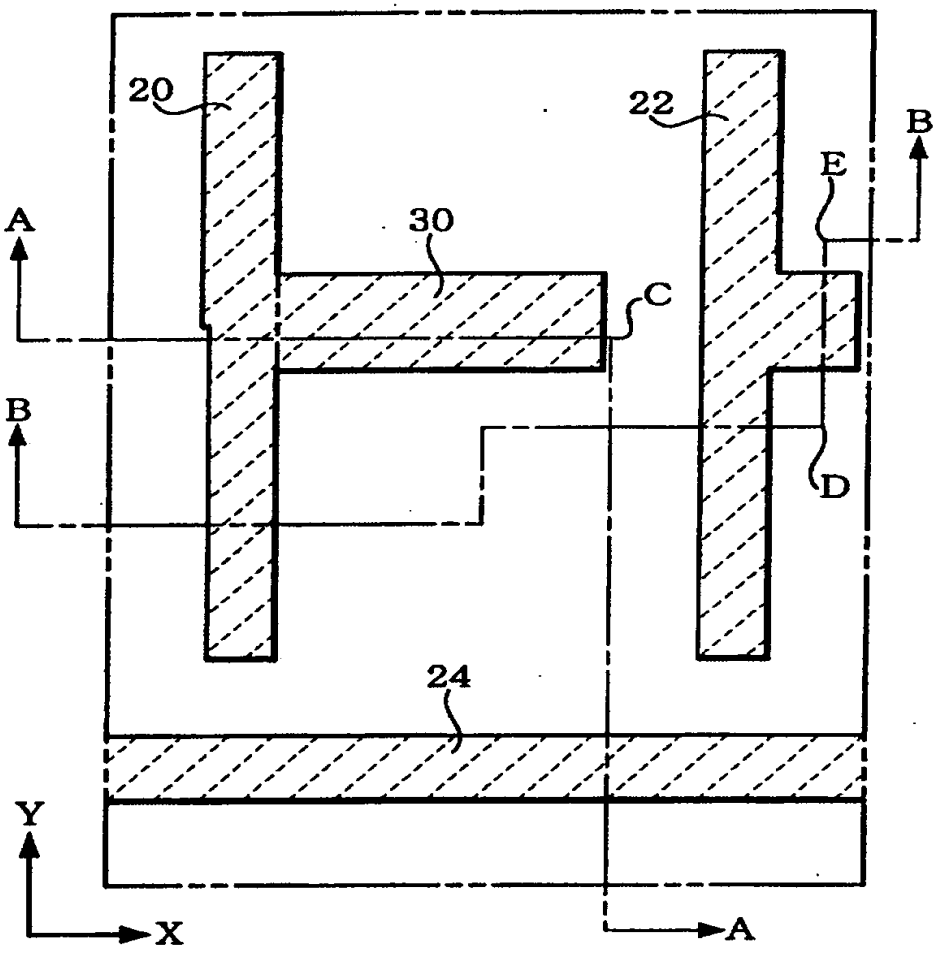


Fig. 4

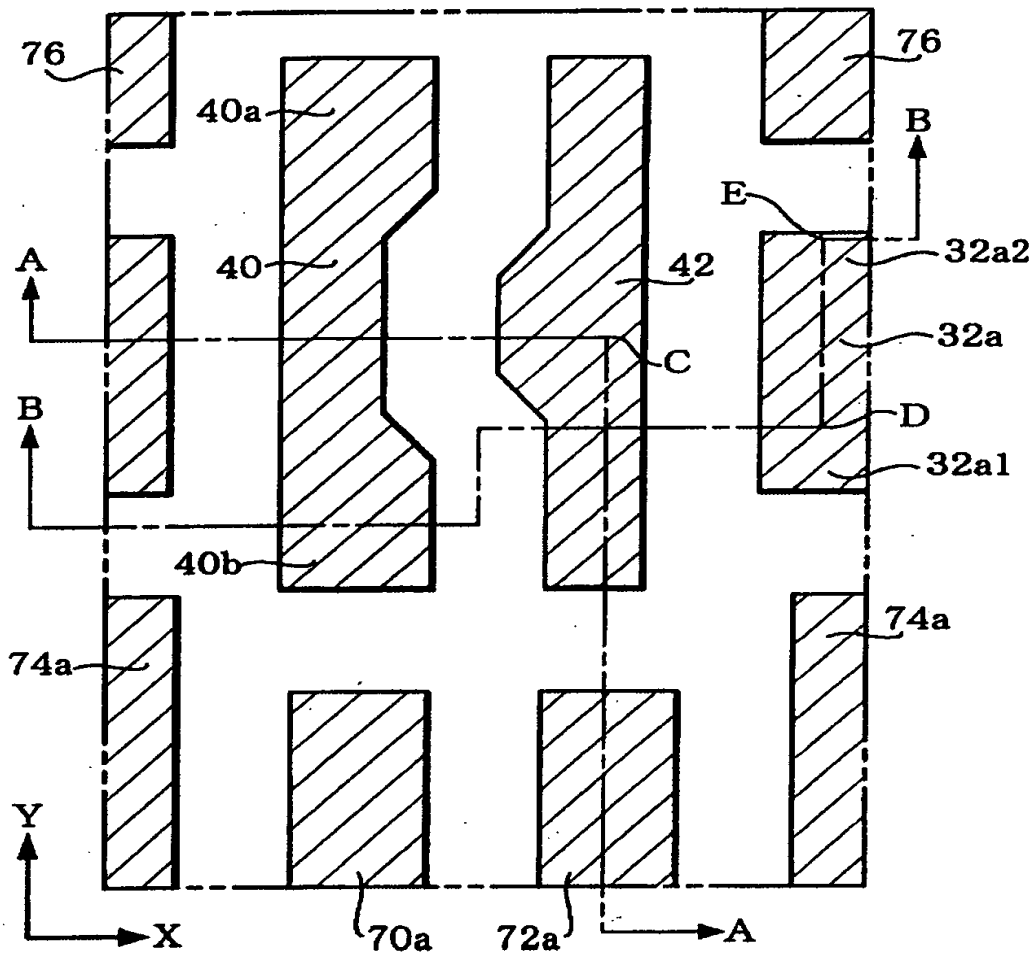

Second conductive layer
76
40a
76
B
E
A
40
42
32a2
32a
C
B
D
32a1
40b
74a
74a
Y
X
70a
72a
A

Fig. 5

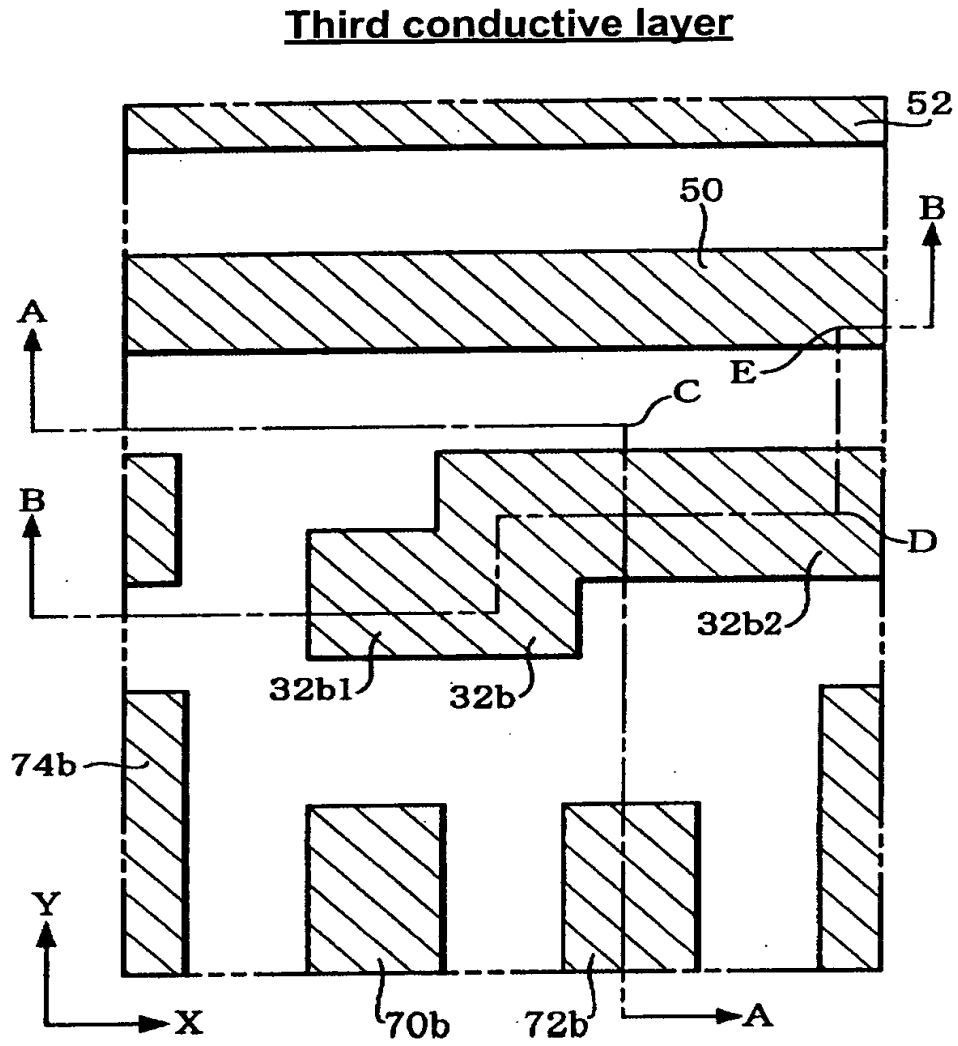

Third conductive layer
52
50
B
A
E
C
B
D
32b2
32b1
32b
74b
Y
X
70b
72b
A

Fig. 6

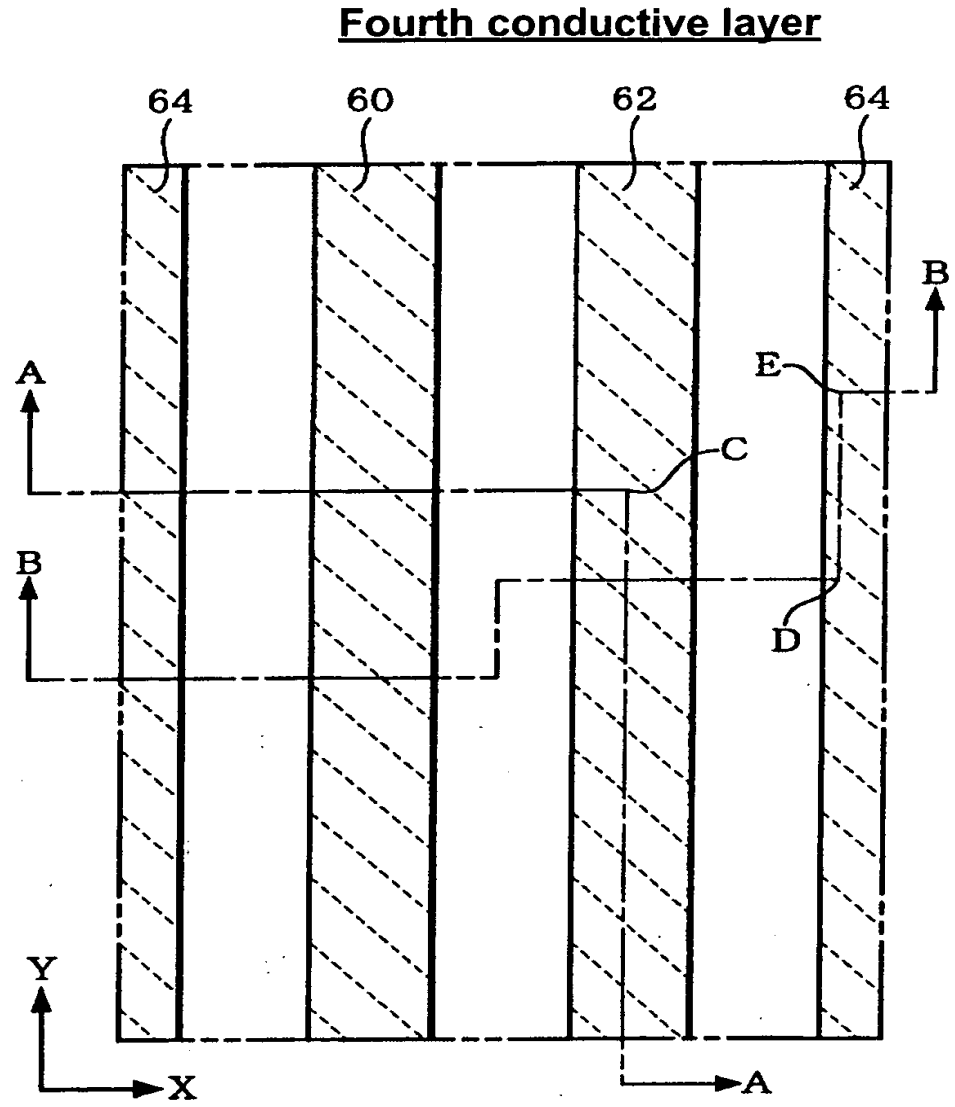


Fig. 7

Field / First conductive layer

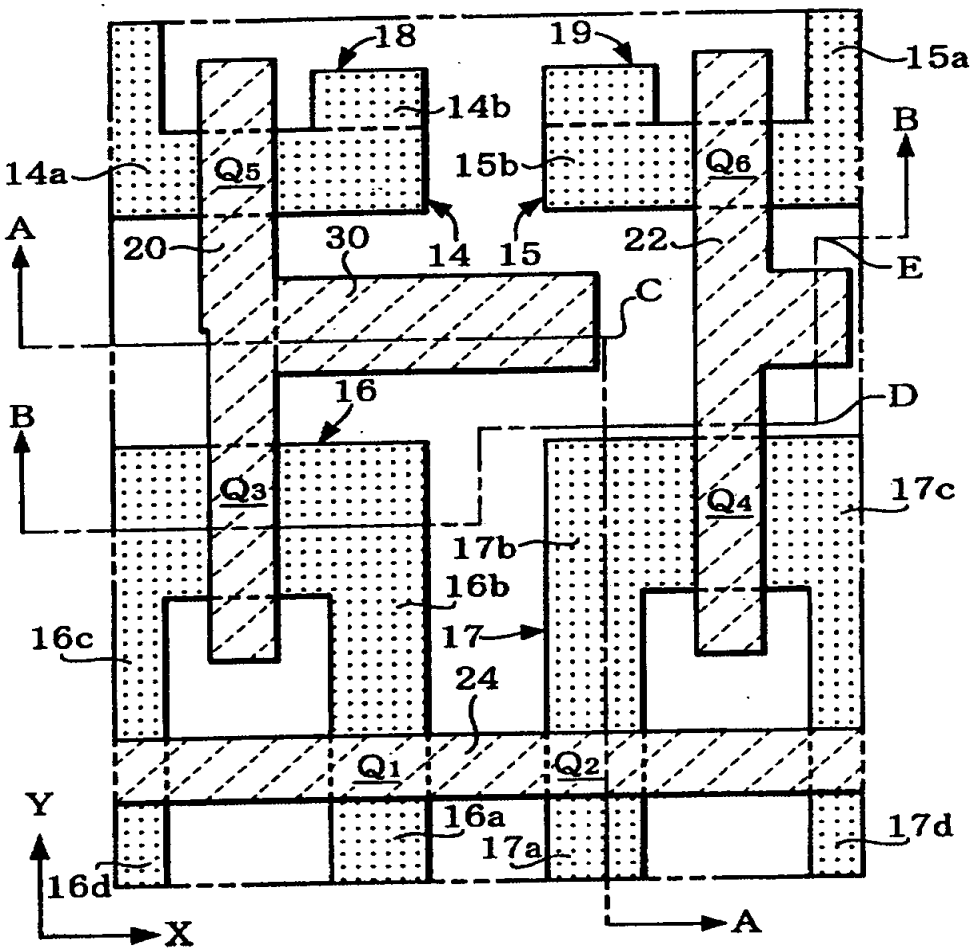


Fig. 8

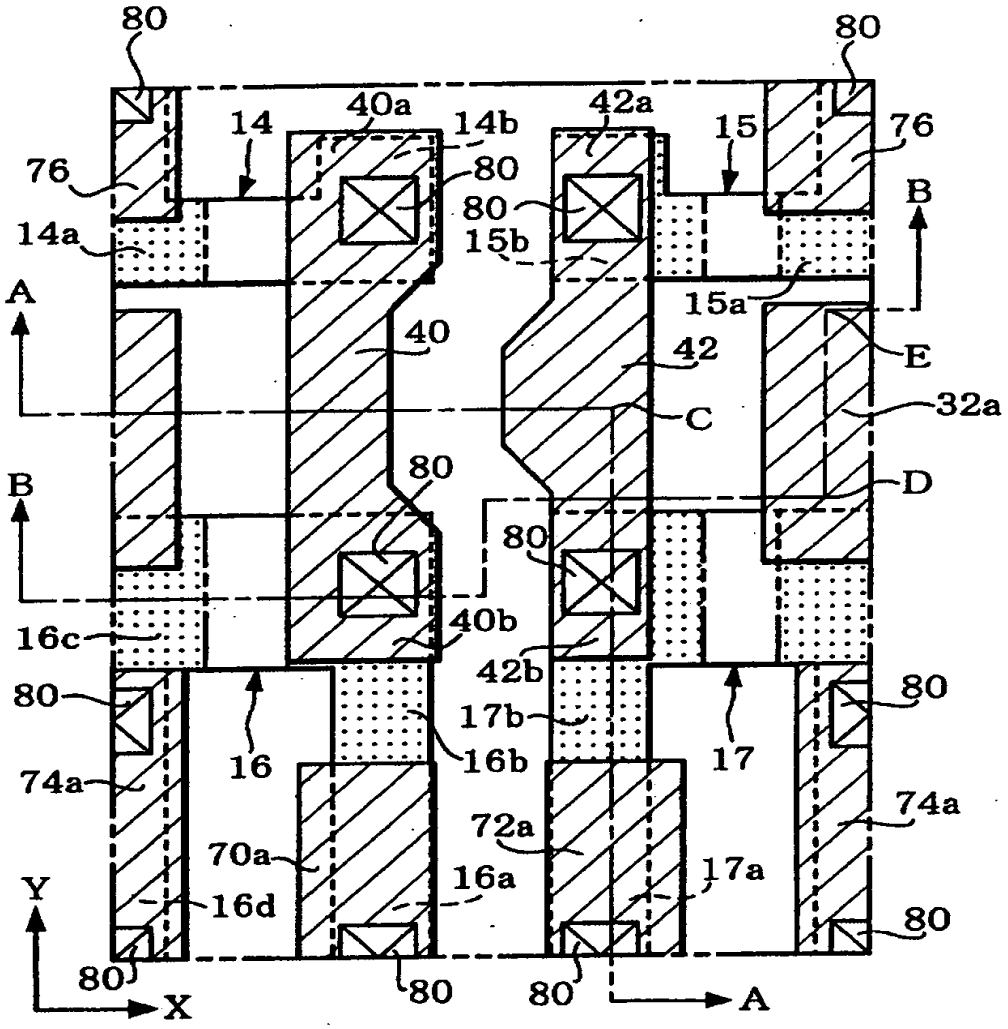

Field / Second conductive layer
80
80
14
40a
14b
42a
15
76
76
80
80
B
14a
15b
A
15a
40
42
E
C
32a
80
B
D
80
16c
40b
42b
80
80
17b
16
16b
17
74a
74a
72a
70a
16a
17a
Y
16d
80
80
80
80
X
A

Fig. 9

First conductive layer / Second conductive layer

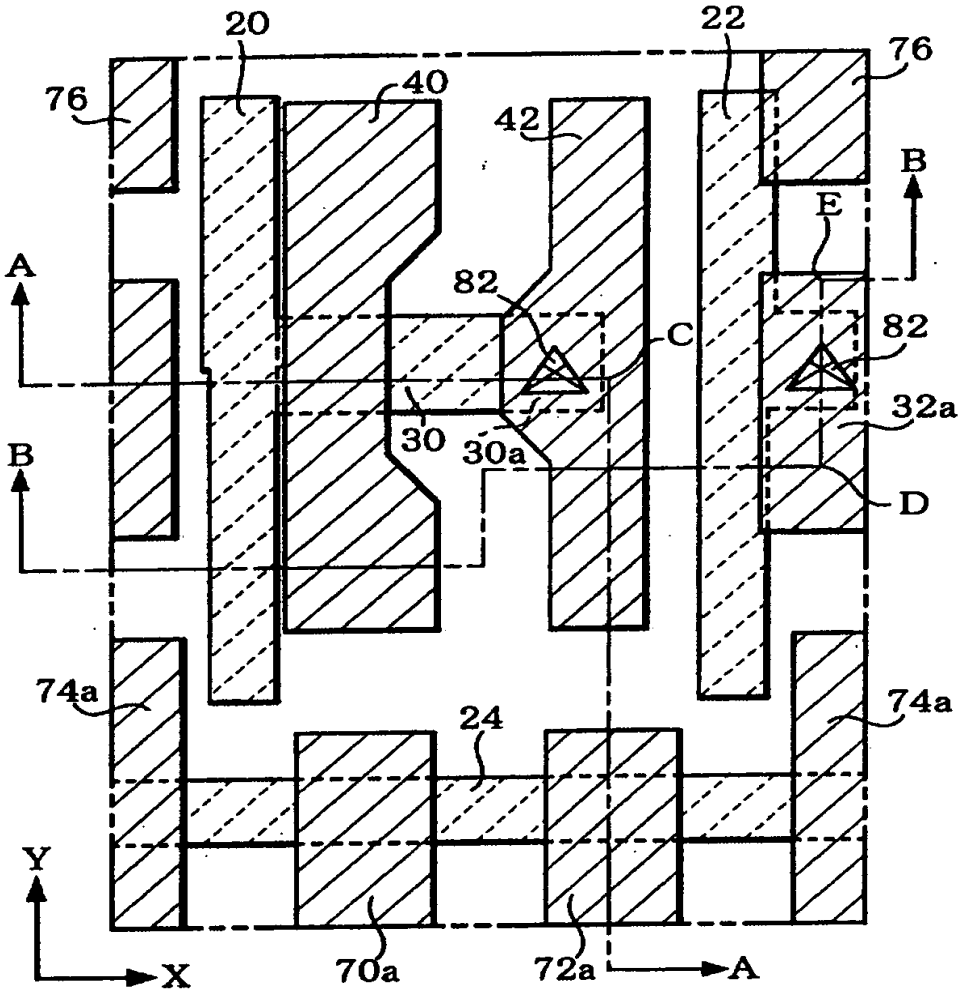


Fig. 10

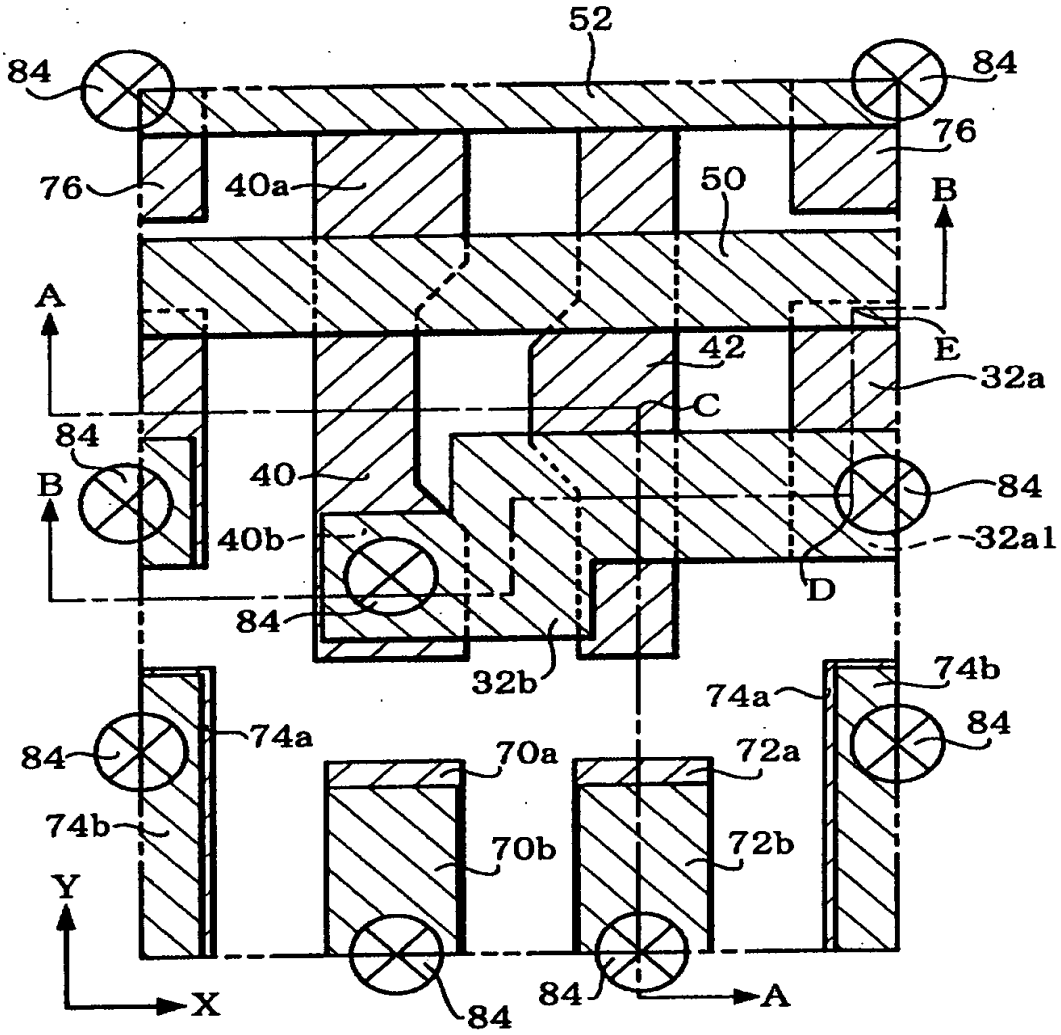
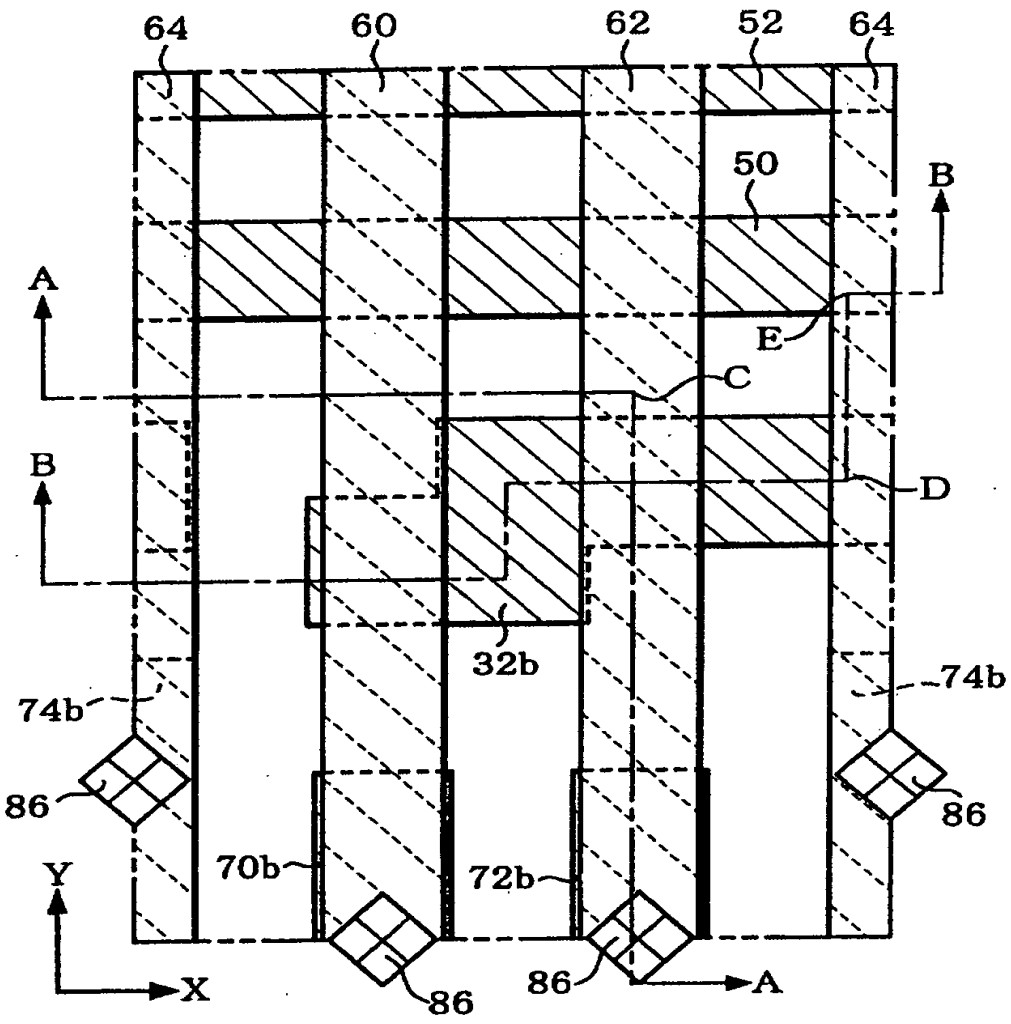

Second conductive layer / Third conductive layer
52
84
84
76
76
40a
50
B
A
42
E
32a
C
84
40
84
B
40b
32a1
D
84
32b
74b
74a
84
74a
84
70a
72a
74b
70b
72b
Y
X
84
84
A

Fig. 11


Third conductive layer / Fourth conductive layer
64
60
62
52
64
50
B
A
E
C
B
D
32b
74b
74b
86
86
70b
72b
Y
X
86
86
A

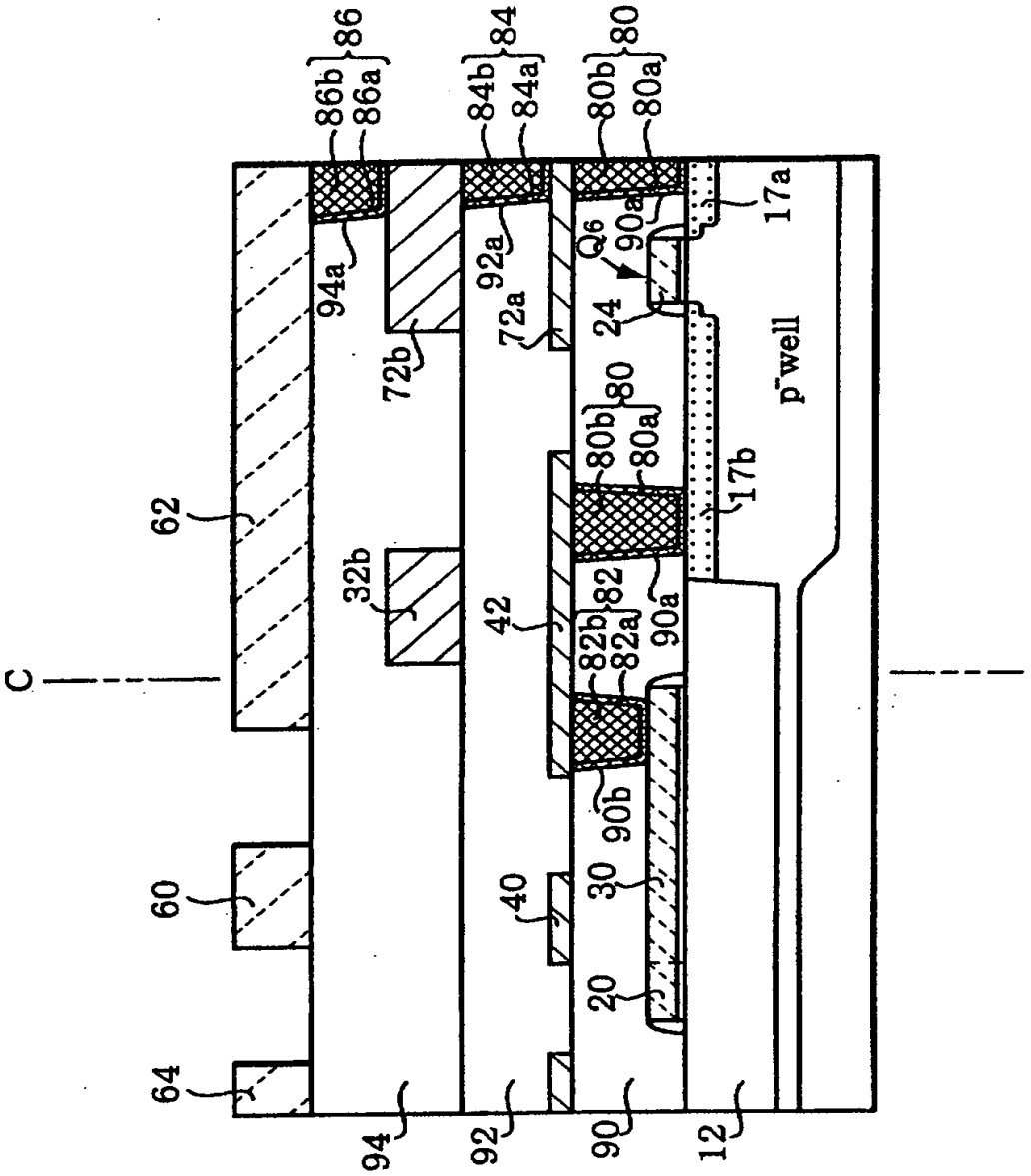

86
86b
86a
84
84b
84a
80
80b
80a
94a
92a
72a
72b
Q6
90a
24
17a
p⁻well
62
32b
42
82
82b
82a
17b
C
60
40
30
90b
20
64
94
92
90
12

Fig. 12

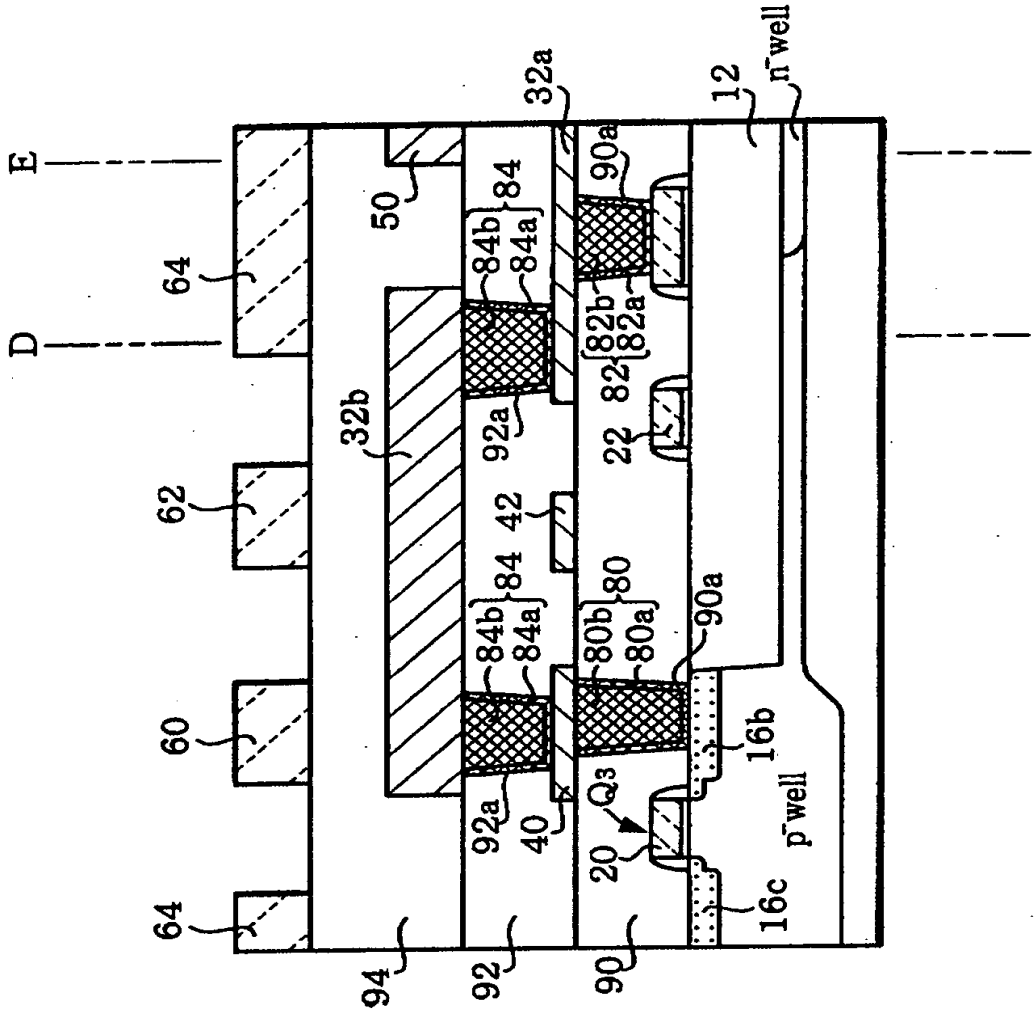

E
D
64
62
60
64
50
32a
32b
84
84b
84a
92a
42
84
84b
84a
92a
40
Q3
20
12
n⁻well
90a
82
82b
82a
22
80
80b
80a
90a
16b
p⁻well
16c
94
92
90

Fig. 13

Fig. 14

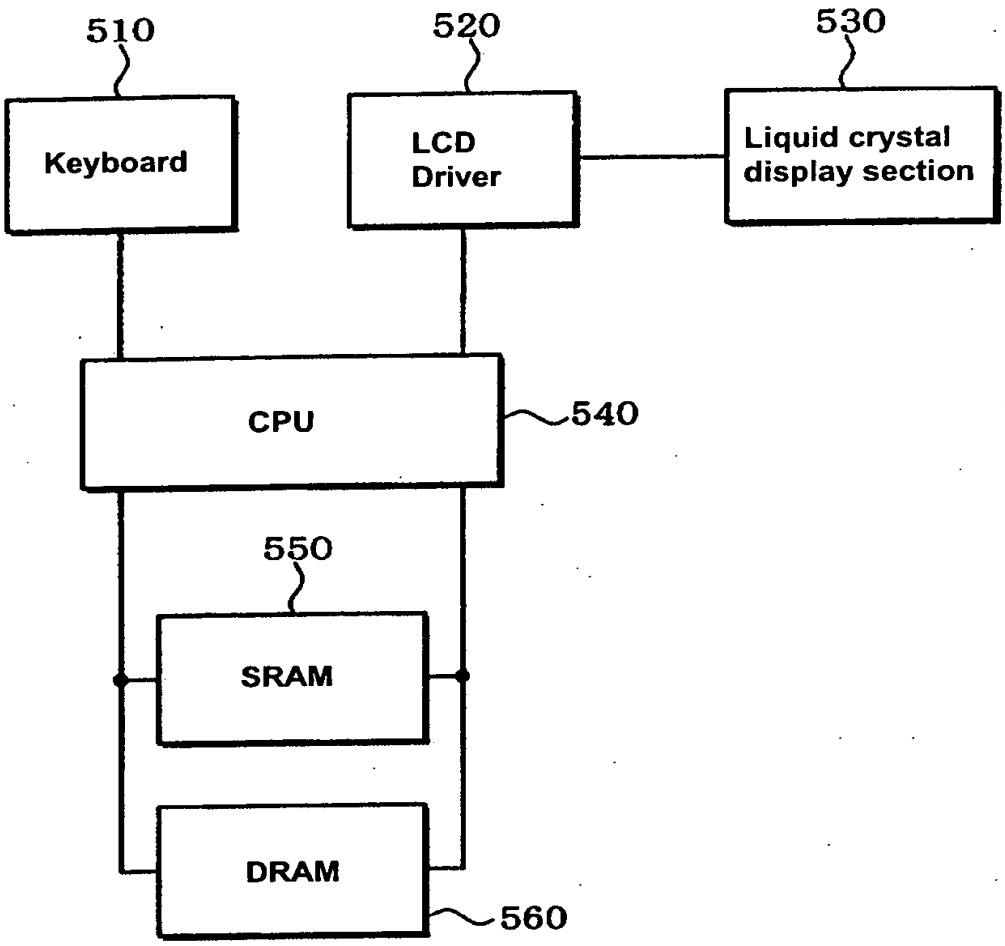

510
520
530
Keyboard
LCD Driver
Liquid crystal display section
CPU
540
550
SRAM
DRAM
560

Fig. 15

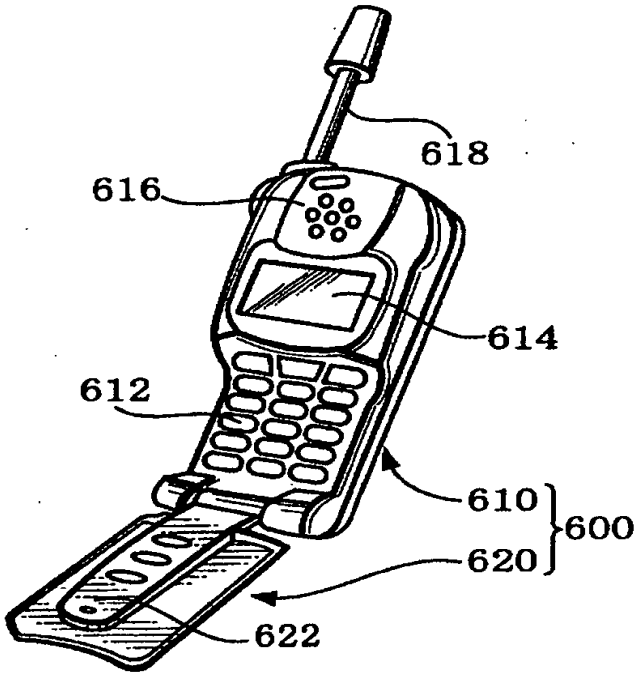


Fig. 16

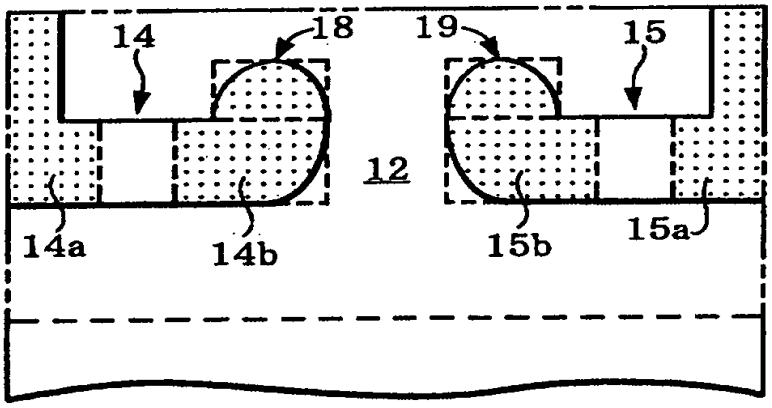


Fig. 17A

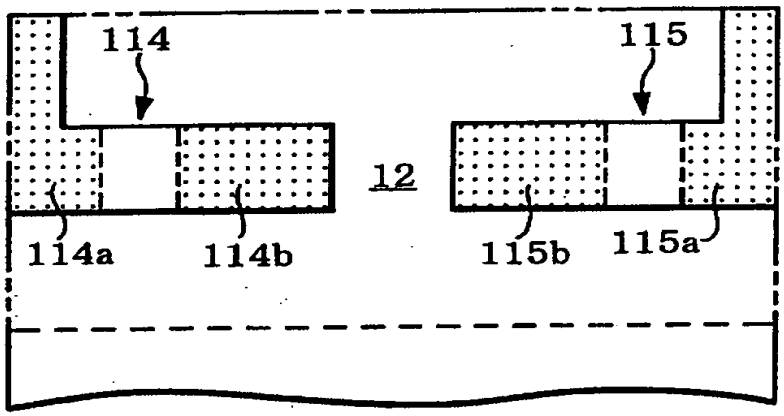
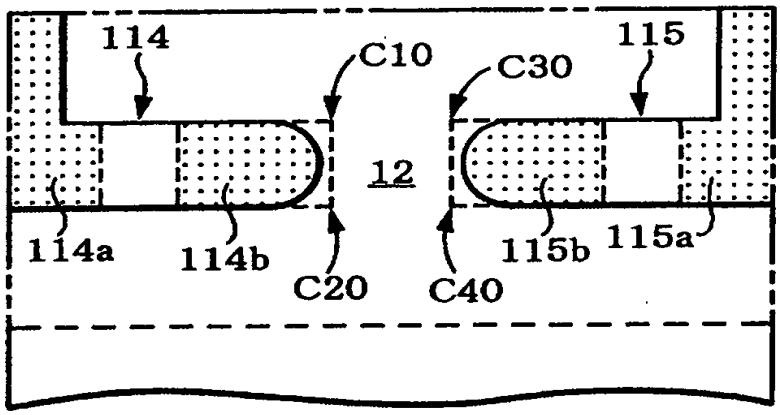


Fig. 17B



[Name of Document] ABSTRACT

[Abstract]

[Object] The present invention provides a semiconductor device that can reduce its cell area. The present invention further provides a memory system and an electronic apparatus that includes a semiconductor device of the present invention.

[Arrangement] A semiconductor device is provided with an SRAM memory cell. The semiconductor device includes a first gate-gate electrode layer 20, a second gate-gate electrode layer 22, a first drain-drain wiring layer 40, a second drain-drain wiring layer 42, a first drain-gate wiring layer 30 and second drain-gate wiring layers 32a and 32b. The first drain-gate wiring layer 30 and an upper layer and a lower layer of the second drain-gate wiring layer 32a and 32b are located in different layers, respectively. A first protruded active region 18 is provided in a manner to protrude from an end portion of the first active region 14.

[Selected Figure] Fig. 2